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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,050	01/29/2002	David R. Blythe	1026.00	3659

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EXAMINER	
LAY, MICHELLE K	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,050	BLYTHE ET AL.	
	Examiner	Art Unit	
	Michelle K. Lay	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims **1**, **2**, **6**, **8 – 10**, are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. US 6,344,852 B1 to Zhu et al.

Zhu et al. discloses a system and method implemented in hardware to optimize rendering of a computer graphics image, which may be displayed in an image frame comprising a number of tiles. In regards to claims **1** and **2**, Fig. 1 illustrates a graphics system (10) that operates on graphics data that can be used to produce an image on a display device. The graphics data may be generated by dedicated geometry hardware or a central processing unit of a host computer (claim **2**) [column 3, lines 14 – 15]. Graphics data can include geometry data and mode data. Geometry data comprises information relating to various geometries (e.g., triangles, parallelograms, rectangles, circles, etc.) that can be processed to produce a complete image (claim **2**) [column 3, lines 19 – 24]. Fig. 3 illustrates an exemplary frame (38) in which an image can be displayed (claim **1**) [column 12, lines 1 – 2]. This frame is considered the compositing window as claimed. Frame (38) comprises or is divided into a number of regions or tiles

(40) (claim **1**). Tiles (40) can be organized into nxm array in frame (38) [column 12, lines 2 – 7]. These tiles are considered the subareas as claimed. Each tile (40) may comprise one or more picture elements ("pixels"), which also may be organized in an array. A portion of the overall image is displayed in each tile (40) [column 12, lines 10 – 14]. One or more geometries, such as exemplary geometry (42), may be generated on frame (38). Each geometry (42) may be contained in or touch one or more titles (40). Each geometry (42) can be a polygon having three or more vertices (44), such as exemplary vertices (44a), (44b), and (44c) [column 12, lines 19 – 24]. The geometries within each tile are considered the geometry chunks as claimed where the bounding region is the region within the tiles (claims **1**, **2**).

In regards to claim **6**, a binning engine (12), which is implemented in hardware separate from a host computer, receives the graphics data. Using the graphics data, binning engine (12) virtually reproduces the associated geometries and modes in an image frame that comprises a number of distinct regions referred to as tiles. Binning engine (12) determines which tiles are "touched" by each geometry. For every tile, the graphics data for each geometry touching the tile is linked to that specific tile [column 3, lines 43 – 52].

Regarding to claims **9**, **10**, Fig. 2 is a block diagram for an exemplary embodiment of binning engine (12). Binning engine (12) generally functions to selectively bin graphics data into the various memory bins (18) [Fig. 1]. In particular, binning engine (12) operates on graphics data to determine which tiles in an image frame are touched by each geometry specified in and/or further defined by the graphics data; from this,

binning engine (12) outputs synchronized graphics data packets (14) for storage into memory bins (18), each of which is specific to a particular tile [column 5, lines 25 – 39]. The graphics data may be generated, and/or sent, by a CPU or dedicated geometry processing hardware. Graphics data comprises information that can be used to generate or produce an image. The Z-stream contains vertex (e.g., X, Y, Z coordinates) data for various geometries along with some mode data. Such vertex data can be linked according to primitives formed from the geometries (claim **9**) [column 5, lines 47 – 50]. As depicted in Fig. 2, the binning engine (12) includes a geometry buffer (22). A vertex buffer (26), which is coupled to geometry buffer (22), comprises a queue to buffer vertices for one or more polygons defined by the geometry data (claim **10**) [column 6, lines 15 – 17].

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1**, **3 – 5**, **7**, **8**, **11**, **15 – 19** are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,104,842 to Rich.

Rich discloses a method, apparatus and computer program for transforming from model to screen coordinates by assigning specified subsets of the plurality of parallel processing elements respective model space geometric primitives. In regards to claim **1**, **8**, and **19**, the image generation system (20) illustrated in Fig. 1 is provided with

object models by a controlling process executing in the host processor (22) that selects object models as necessary, and provides a list of objects (claims **8**, **19**) to the image generation system (20) [column 6, lines 18 – 19]. Referring to Figs. 3, 4, and 5, a database of model elements that comprise the screen image to be generated is constructed by the host processor in model coordinates. The image generation system then carries out four functions to convert the model in the database to an image in the frame buffer. These four functions are geometric processing, rasterization, shading/texturing and composition [column 8, lines 15 – 20]. After each of the desired operations reflected in block (52) have been carried out, the processing elements (32) write the list of transformed primitives to external memory in clock (53) [column 8, lines 53 – 54]. Because the screen is divided into a number of regions (claim **1**), a list for each region is generated which lists the primitives (claim **1**) that touch that region. This list is written to external memory as seen in block (54) [column 8, lines 59 – 62]. These regions are considered the claimed subareas and the primitives the geometry chunks where the bounding region is the area that the primitives are located in. A frame is a complete set of information required to provide a screen with enough data to present visual information (claim **1**) [column 6, lines 14 – 15]. This frame is considered the compositing window as claimed.

Regarding claims **3** – **5**, Fig. 1 illustrates an integrated image generation system (20) that communicates with a host processor (22), video memory (24) and a display device (26). The integrated image generation system (20) receives information from the host processor (22) from which the image generation system (20) generates an image

to be displayed on the display device (26) [column 5, lines 43 – 49]. A software model of objects to be displayed is created with the host processor (22). An object is a two or three dimensional software model of a thing that is to be displayed. Objects may be composed of polygons, which are portions of planes defied by three or more vertices in a three dimensional coordinate system (claim **5**, **17**) [column 5, lines 51 – 55]. The polygons of the object models may be defined in a three-dimensional space, often called "world" or "model" coordinates, and texture patterns or "texture maps" are defined in a two-dimensional space for each pattern (claim **4**, **16**). The image generation system (20) receives or obtains models generated by the host processor (22) and operates on those models to create an array of picture elements of "pixels" which are in two-dimensional space referred to as "x-y space" or "screen coordinates (claim **3**, **15**) [column 6, lines 1 – 5].

In regards to claims **7**, **11**, illustrated in Fig. 2, the image generation system (20) includes a plurality of processing elements (32), which make up a processing element array (30). These processing elements (32) operate as a single instruction, multiple data processing array so that the same processing instruction is supplied to multiple individual processors, but each processor operates on a different data stream [column 6, lines 38 – 46]. Each processing element (32) is assigned to a separate pixel (claim **7**) [column 6, line 68]. The processing element array element control unit (40) is primarily responsible for sequencing instructions and address to the processing element array (30) (claim **11**) [column 7, lines 1 – 3]. Referring to Fig. 16B, a region (132) is shown to be divided into four subregions (136). In the present example, each

subregions (136) comprises a two dimensional array of 16 pixels wide and 16 pixels deep. The regional and subregional organizations as shown in Figs. 16A and 16B are based upon a processing element hardware allotment of 256 [column 27, lines 62 – 68] processing elements, however, other numbers of processing elements and region dimension may be utilized (claims **11**, **18**) [column 28, lines 1 – 2].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **11 – 14**, **20**, **21** are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. US 6,344,852 B1 to Zhu et al.

Zhu et al. teaches the claimed limitations of claims **11 – 14**, expect specifying multiple graphics units. However, it would have been obvious at the time the invention was made to allow multiple graphic units to perform the same operation as the graphic unit that is disclosed by Zhu et al. because if one or more units are not available, the remaining functional units may still perform so that delay does not exist.

Zhu et al. discloses a system and method implemented in hardware to optimize rendering of a computer graphics image, which may be displayed in an image frame comprising a number of tiles. Referring to Fig. 1, a binning engine (12), which is implemented in hardware separate from a host computer, receives the graphics data

(claim **12**) [column 3, line 45]. It would have been obvious that the binning engine (12) includes a unit, such as the virtual graphics unit as claimed, so that the binning engine (12) has a means of receiving this graphics data (claim **13**). The graphics data may be generated by dedicated geometry hardware or a central processing unit of a host computer (claim **14**) [column 3, lines 14 – 15]. Graphics data can include geometry data and mode data. Geometry data comprises information relating to various geometries (e.g., triangles, parallelograms, rectangles, circles, etc.) that can be processed to produce a complete image (claim **14**) [column 3, lines 19 – 24]. Using the graphics data, binning engine (12) virtually reproduces the associated geometries and modes in an image frame that comprises a number of distinct regions referred to as tiles. Binning engine (12) determines which tiles are "touched" by each geometry. For every tile, the graphics data for each geometry touching the tile is linked to the tile (claim **11**) [column 3, lines 43 – 52]. This binning engine (12) is considered the geometry distributor. As explained in claim 1, the tiles are considered the claimed subareas where the region of each tile is defined as the bounding region and the data within this region are the geometry chunks. A rendering engine (20) is coupled to memory bins (18). In general, rendering engine (2) accesses the graphics data contained in memory bins (18) to render an image for display. With the graphics data stored into separate memory bins (18) for each tile of an image frame, rendering engine (2) can readily retrieve graphics data from each bin (18) to render the relevant portion of an image within the respective tile of a frame (claim **11**) [column 4, lines 56 – 64].

Regarding to claims **20**, **21**, Fig. 2 is a block diagram for an exemplary embodiment of binning engine (12). Binning engine (12) generally functions to selectively bin graphics data into the various memory bins (18) [Fig. 1]. In particular, binning engine (12) operates on graphics data to determine which tiles in an image frame are touched by each geometry specified in and/or further defined by the graphics data; from this, binning engine (12) outputs synchronized graphics data packets (14) for storage into memory bins (18), each of which is specific to a particular tile [column 5, lines 25 – 39]. The graphics data may be generated, and/or sent, by a CPU or dedicated geometry processing hardware. Graphics data comprises information that can be used to generate or produce an image. The Z-stream contains vertex (e.g., X, Y, Z coordinates) data for various geometries along with some mode data. Such vertex data can be linked according to primitives formed from the geometries (claim **20**) [column 5, lines 47 – 50]. As depicted in Fig. 2, the binning engine (12) includes a geometry buffer (22). A vertex buffer (26), which is coupled to geometry buffer (22), comprises a queue to buffer vertices for one or more polygons defined by the geometry data (claim **21**) [column 6, lines 15 – 17].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. US 6,219,058 B1 to Trika.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle K. Lay whose telephone number is (571) 272-7661. The examiner can normally be reached on Monday - Friday, 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mkl 03.25.2005

4/1/05

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